L2beta WBS 1.2.4

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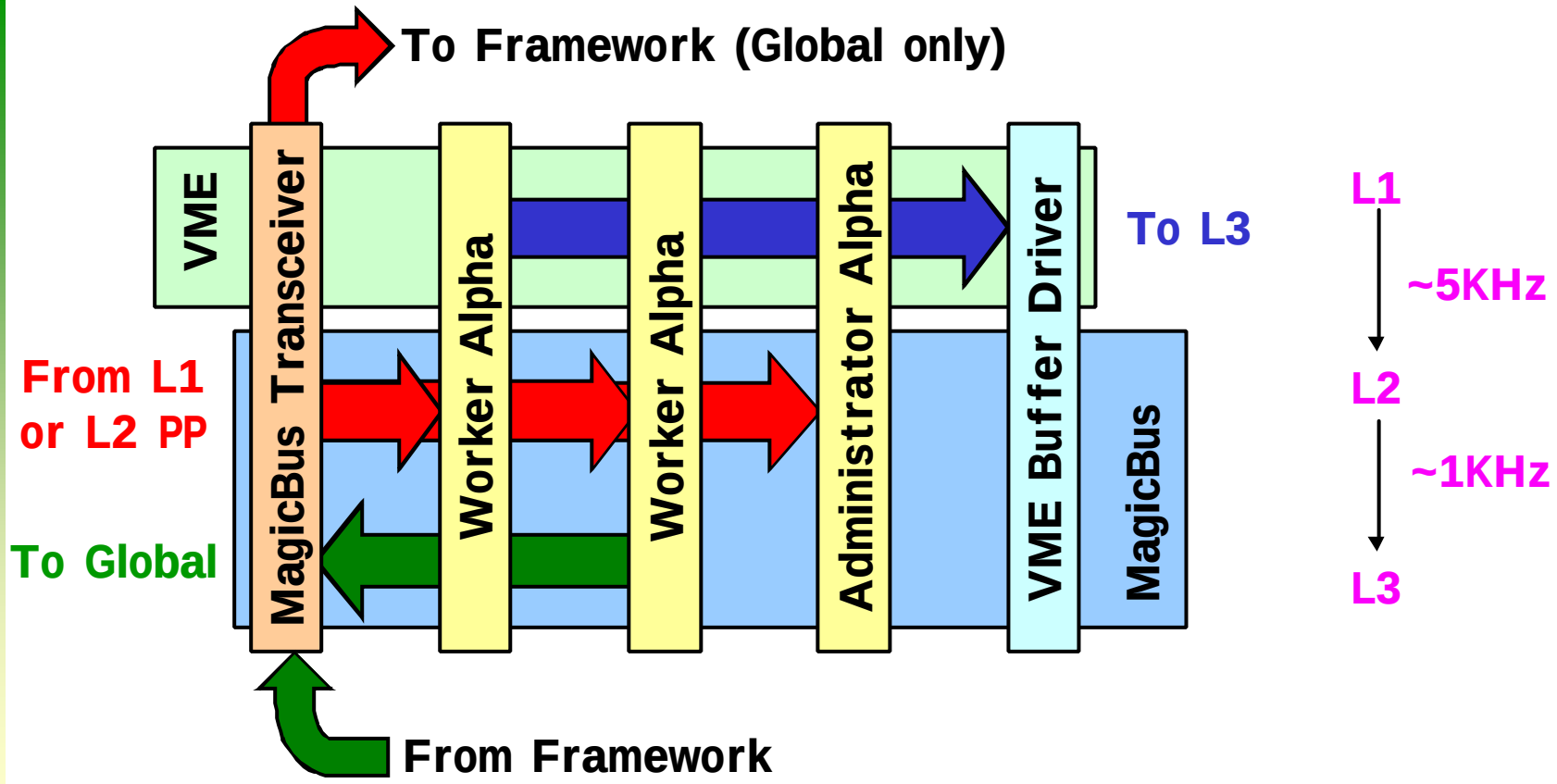
L2beta Intro

- The L2Alpha/beta processors in conjunction with other hardware provide processing power for data clustering for each D0 detector subsystem.
- All subsystems output to GLOBAL processor crate that makes event wide correlations between the subsystem clusters and matches these data against programmable trigger criteria.

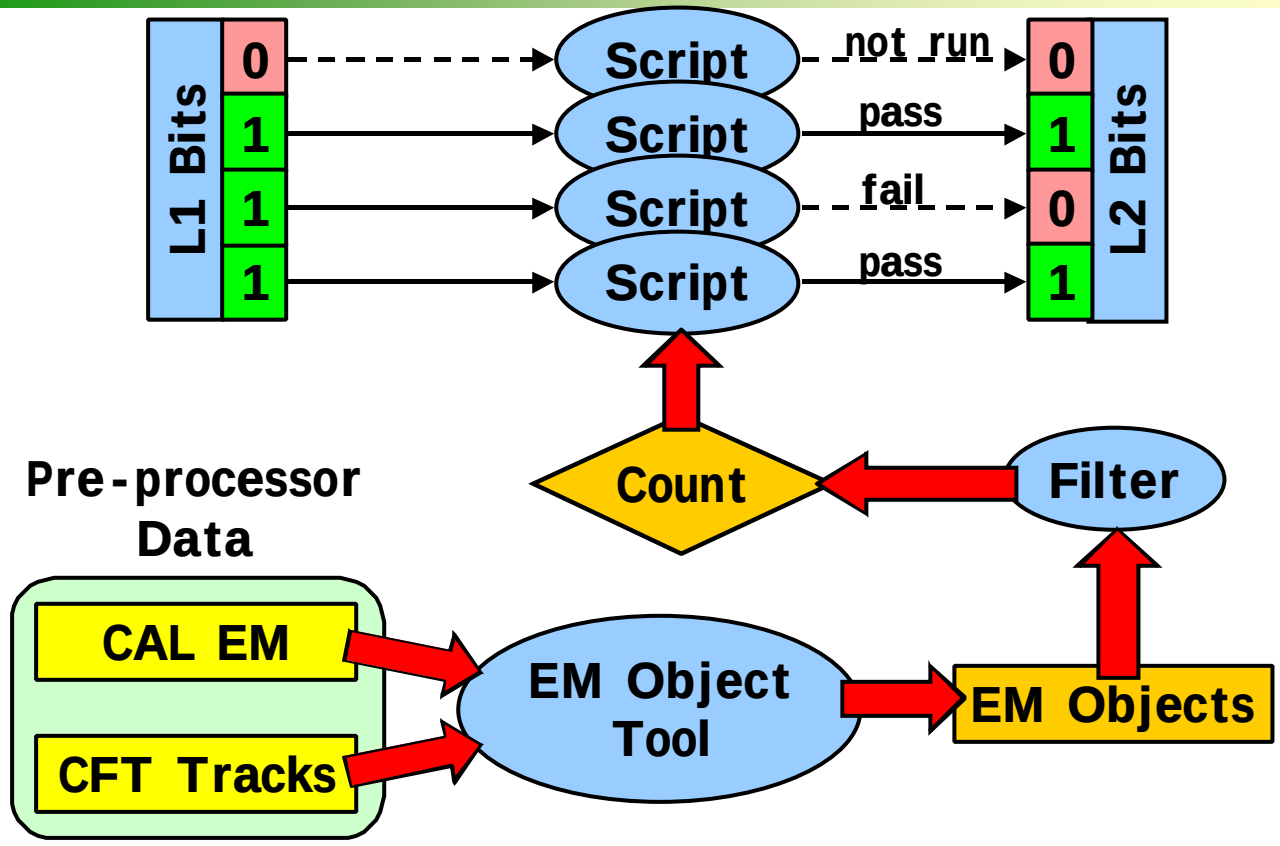
- Over the next few months, D0 plans to retire Alpha processors and instrument the trigger with a complete set of betas.
- The beta processors have been designed to be easily upgradeable to higher performance CPUs.

L2processor Dataflow



L2Global Dataflow

L2 Global



L2 Current Processing Time on L2Alpha Processors

Zero Bias Run, Maxopt Timing

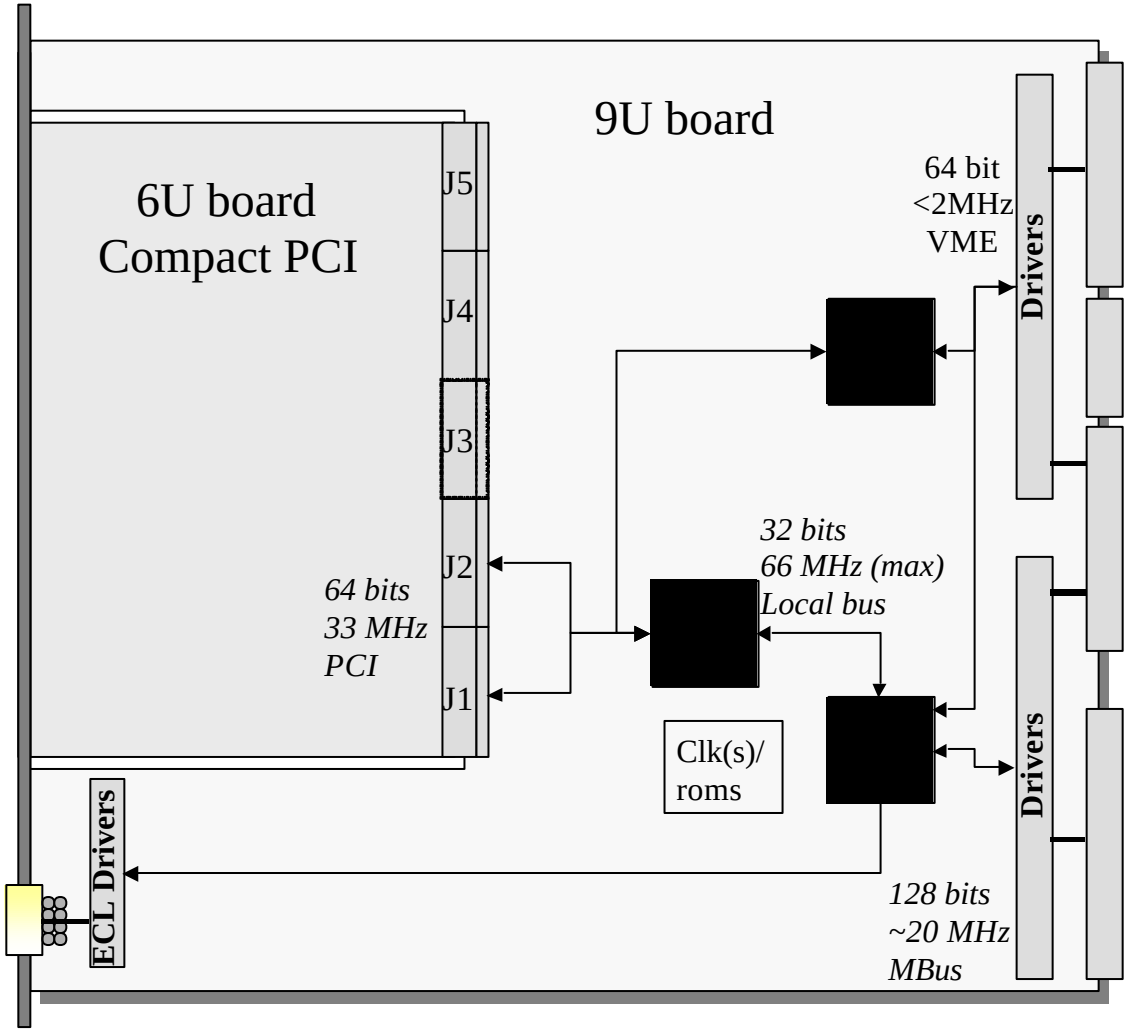
Pre-Processor	Total Time (ms)
L2GLobal (with inputs below)	230
L2Central Muon	132
L2Forward Muon	81
L2Calorimeter (combined, 6inputs)	187

Target timing ~50ms /stage

Add ~20% for current triggerlist

L2beta Block Diagram

- PIII Compact PCI card
- 9U card with "custom" devices (3 BGA's)
  - –Universe Chip VME interface
  - –commercial 64-bit PCI interface chip
  - –MBus and other logic in FPGA



L2beta vs Alpha CPU

I/O Performance	
Alpha	~100 MB/s
MBT	~160 MB/s
L2beta	~250 MB/s
SBC	~500 MB/s

Cheap upgrade = add 2nd CPU*

CPU/MHz	Specint95	Specfp95
Alpha/500	~15	~21
PIII/850	~41	~35
PIII/1000	~48	~41

*but SW not trivial

L2beta Prototype

Prototypes debugged/verified beginning of June

1st preproduction series board shipped from Orsay last week

Beta Group

Virginia: design, hw/fw specs, debugging, software, Alpha transparency

Orsay: design, engineering, debugging, firmware

UMD: design, fw consultation

Run2b L2beta Requirements

In Run2b, the input and output rates will remain fixed for L2 at around 5KHz and 1KHz respectively.

The L2 processors will therefore be required to maintain the same level of rejection as in Run2a, despite moving a significant amount of rejection upstream to L1 and working in a higher luminosity environment.

L2beta Upgrade

Upgrading the processors poses little technical risk. To 1st order processors are simply swapped out of 9U mother cards.

A small, passive adapter may need to be built for hard drive connections.

Minor firmware updates may be necessary for optimal functioning in the Run2b trigger.

Sample L2beta Algorithms

Examples of upgraded processing:

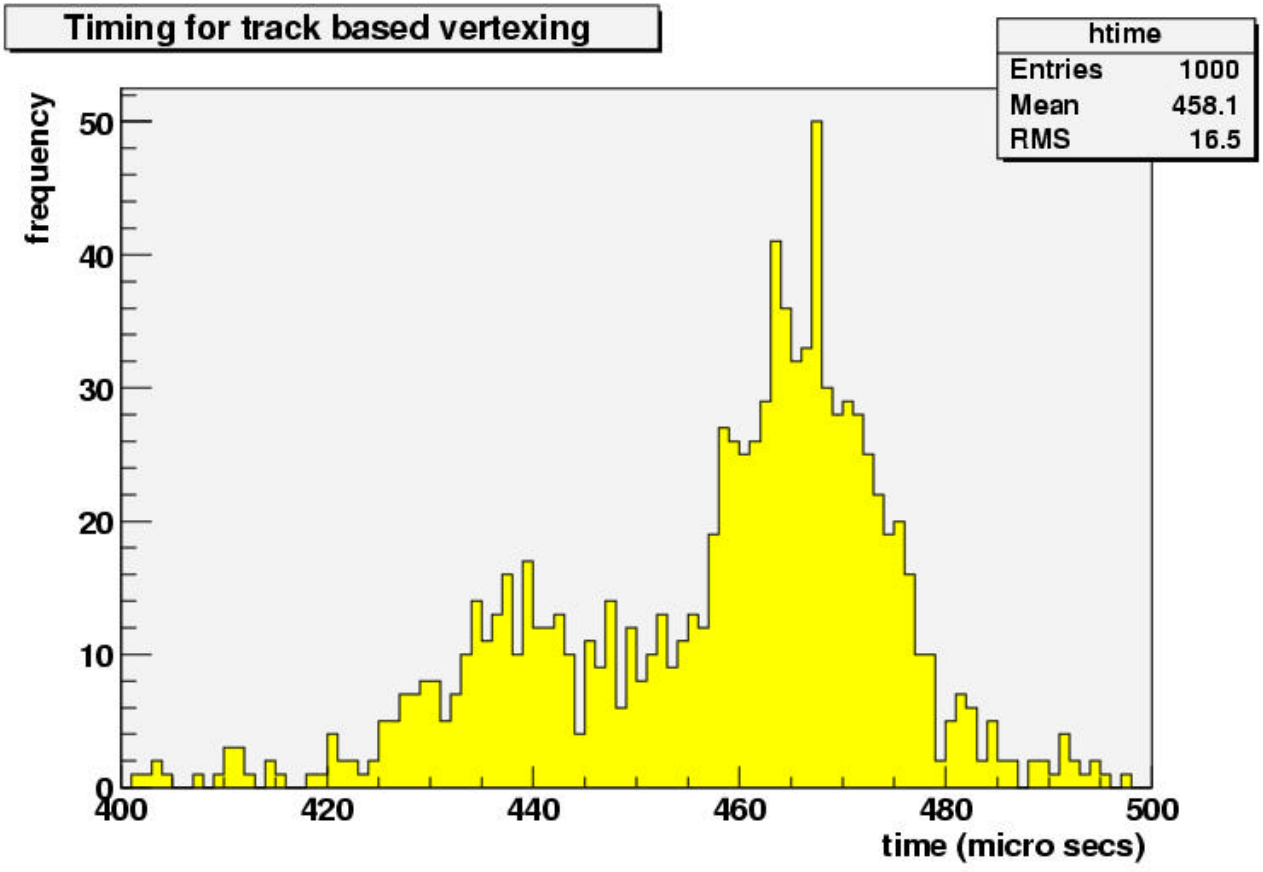
- **Add vertex information to sharpen calorimeter triggers (30-60%) rate reduction for jet triggers (Eta dependent) with ~10cm vertex resolution.**

Requires passing rough Z information along w/ STT tracks and application of track-based vertex finder.

L2beta Vertexing

Timing for track-based vertex finder in L3 using 1.5GHz CPU

Such algorithms will be accessible at L2 as CPU performance increases and by parallelizing work between nodes…



L2beta Sample Algs. (cont)

Examples of upgraded processing (cont):

- **Multi-track displaced vertices**

Requires passing rough Z information along w/ STT tracks, use CTT or Global processor to correlate Z sectors with Phi/impact parameter(significance). Adds linearly to processing time, but offers advantage if impact parameter significance can be held lower at STT.

L2beta Sample Algs. (cont)

Examples of upgraded processing (cont):

- **Sharpen calorimeter resolutions through application of improved calibrations at L2. Current processors would at 35-70us to processing time complete this task.**
- **Develop NN scheme for improved t recognition, etc**
- **Other L3 algorithms for porting…**
- **Trigger branching at L2 Global**

L2beta CPU Breakdown

Upgrade 12 CPUs to fastest available for Run2b. Breakdown of new CPU locations and new functions:

- **Calorimeter (2 CPU) - apply data corrections to improve ET resolution jets, electrons, Missing ET**
- **Global (3) – Apply vertex corrections to calorimeter objects, improve b-tagging by searching for multi-track displaced vertices. Enhanced trigger branching.**
- **Tracker (2) – Handle increased number of silicon layers, calculate quantities needed for z-vertex and multi-track displaced vertices**
- **Muon (1) - Maintain rejection at high occupancy.**
- **Preshower (2) – Maintain rejection at high occupancy.**
- **Spare/test (2) – spare + "shadow" node for test/development purposes**